Notice of Allowability	Application No.	Applicant(s)	
	10/736,722	PARK, KI CHON	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 9/16/2005*.

2. ☒ The allowed claim(s) is/are *1-5,7-14 and 16-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 01/10/2005
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

Response to Amendment

1. The amendment received on 9/16/2005 has been received and entered in the case. The prior art rejections to the claims made in the previous Office Action, mailed on 7/13/2005, are now withdrawn in view of Applicant's amendment. Therefore, the case is now found to be in allowance condition as set forth below.

REASON FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose or fairly suggest circuit for generating an internal clock signal (as shown in Fig. 3) and a method of use thereof, as recited in claims 1 and 15, having specific structural limitations such as an internal clock signal generator comprises a delay unit for delaying the external clock signal by some time; and a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a circuit for generating an internal clock signal, as recited in claim 7, having specific structural limitation such as a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock

signal as it is, the pulse-shaping unit comprising a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the detecting signal of the operating frequency decision unit; a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted; and an inverter for inverting the output signal of the second NAND gate; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest circuit for generating an internal clock signal (as shown in Fig. 3) and a method of use thereof, as recited in claims 14 and 18, having specific structural limitations such as an internal clock signal generator for generating an internal clock signal by waveform-shaping the external clock signal, or for outputting the external clock signal as the internal clock signal so that the internal clock signal has the same pulse width and the same frequency as the external clock signal, in response to the detecting signal, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest circuit for generating an internal clock signal (as shown in Fig. 3) and a method of use thereof, as recited in claim 16, having specific structural limitations such as the CAS latency has a value of 0 to 7 and the operating frequency decision unit generates the detecting signal if the value of the CAS latency is over 4, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
September 24, 2005